RANI RASHMONI GREEN UNIVERSITY

Post Graduate Department of Computer Science

M.Sc. Semester-I Supplementary Examination 2024 Subject: Computer Science

Paper: MSCCS101 (Advanced Computer Architecture)

Time: 2 Hours **Full Marks: 40**

The figures in the margin indicate full marks.
Candidates are required to give their answer in their own words as far as practicable.

Group A

1. Answer any five questions **2 X 5 = 10**

(i) Describe at least four characteristics of MIMD multiprocessors that distinguish them from multiple computer systems or networks.
(ii) What is super scaler technology?
(iii) What is vector stride?
(iv) How many address bits are required for a 1024 x 8 memory?
(v) What is the use of Program Counter? How can it be used to handle branch illustration?
(vi) A given memory chip has 12 address pins and 4 data pins. How many number of locations does it has?
(vii) "Dynamic pipeline is always multifunction" – Justify the statement.

Group B

[Attempt any five questions]

5 X 6 = 30

2. Consider the following reservation table for a 4-stage pipeline with a clock cycle t = 20 ns.

1	2	3	4	5	
x				x	S1
	X		x		S2
		x	x		S3

(i) What are the forbidden latencies and the initial collision vector?
(ii) Draw the sate transition diagram for scheduling the pipeline.
(iii)Determine the MAL associated with the shortest greedy cycle. 1+3+2=6

3. (a) Explain the concept of Internal Forwarding with respect to a pipelined system.
(b) What are pipeline hazards? 4+2=6

4. Write down matrix (N x N) multiplication algorithm on SIMD (using N number PEs) array processor. Also specify the time complexity with explanation. 5+1

5. Compare between distributed and shared memory architecture of multiprocessor systems with

appropriate diagrams. 6

6. What is the cache coherence problem in a multiprocessor system? Give a solution to this problem. 3+3

7. Explain the difference between three address, two address and one address instruction for the given expression: X=(A+B)*(C+D). 6

8. Differentiate between RISC and CISC architecture. How might single cycle instruction execution be achieved using pipelining? 3+3