RANI RASHMONI GREEN UNIVERSITY
Post Graduate Department of Computer Science

M.Sc. Semester-I Examination 2025
Subject: Computer Science
Paper: MSCCS101(Advanced Computer Architecture)

Time: 2 Hours **Full Marks: 40**

The figures in the margin indicate full marks
Candidate are required to give their answer in their own words as far as practicable

Group- A

1. Answer any five (5) questions. **5 x 2 =10**

i. Write functions of ALU and Control Unit.
ii. Differentiate between SRAM and DRAM.
iii. If i) cache access time 150 ns, ii) main memory access time 980 ns, iii) hit ratio 0.9. Calculate average access time.
iv. What are various Page Replacement Process?
v. What are speed-up, efficiency of pipeline processor?
vi. How many address bits are required for a 1024 x 8 memory?
vii. What is the use of Program Counter? How can it be used to handle branch instruction?

Group- B

Answer any five (5) questions. **5 x 6=30**

2. Design 1K*4 memory architecture using 512*2 RAM Chips. Also show the address and data lines. Explain Memory Hierarchy for computer system. 4+2
3. Create multi stage shuffle-exchange omega network for N=8 and explain it. Difference between arithmetic and instruction pipeline. Why does pipeline require? 3+2+1
4. Write characteristics of CISC and RISC. Explain NUMA, UMA model of multiprocessor system. 3+3
5. For execution of Pipeline Processor of a program of 50000 instructions by linear pipeline with clock rate 60 MHz. No of Stages are 7 and one instruction per cycle. So find, speed up, efficiency, throughput of pipeline over non-pipeline processor. Explain Flynn's classification. 3+3
6. What are pipeline hazards? Explain data hazards. What is dynamic networks? 2+2+2
7. Consider the following reservation table for a four-stage pipeline with a clock cycle t=2ns. 1 + 3 + 2

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

i. What are the forbidden latencies and initial collision vector?
ii. Draw the state transition diagram for scheduling the pipeline.
iii. Determine the MAL associated with the shortest greedy cycle.

8. Explain the difference between difference between three address, two address and one address instruction for the given expression: X=(A+B)*(C+D). 6