Rani Rashmoni Green University

M.Sc. in Computer Science Semester Exam

Subject: Computer Science

Course code: COS-101(Advanced Computer Architecture)

FM=40 marks

1. Answer any four out of six questions from the followings: 2×4=8

a) What is memory hierarchy?
b) What is pipeline stalling.
c) List two differences between RISE and CISE architecture.
d) Discuss different addressing mode by citing appropriate examples.
e) State Amdahl's Law, with an emphasis on its significance.
f) Discuss the architecture of an embedded system.

2. Answer any four out of six questions from the following: 4x4=16

a) A signal-processing team has a legacy non-pipelined data path running at its stage times. They redesign it into a 4-stage pipeline with some extra latch delay. The stage durations (ns) are: 120, 85, 100, 75. Latch delay = 15 ns. They must process 2000 signal blocks.
Calculate:

i. **Pipeline cycle time(ns)**
ii. **Non-pipelined execution time per block (ns)**
iii. **Per-task speed up**
iv. **Overall speed up for the 2000-blockrun**

b) Differentiate MIMD and SIMD Processor.
c) Illustrate the differences between RISC and CISC architectures, providing appropriate diagrams.
d) Consider a 5-stage pipeline structure with 16 instructions and a pipeline cycle time of 4 microseconds. Calculate the following: (a) Speed-up (b) Efficiency (c) Throughput.
e) Compare the write-through and write-back strategie sin cache memory.
f) Discuss various embedded system design issue.

3. Answer any two out of four questions from the following: 2x8=16

a) 1.Assume there is 7-stage pipeline structure, and each stage is taking 1 clock cycle. Find out clock cycles are required to complete the instruction set. And also identify the different types of data hazards.

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MULR1,R2,R3
DIV   R4, R1, R6
ADDR7, R4, R8
SUBR9, R2, R6
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2. Explain Cache coherence problem. 6+2

b) 1. Write down the comparison between data flow and control flow computer system.
2. Define Hit Ratio? Consider a system with 2 level caches. Access times of Level 1 cache, Level 2 cache and main memory are 4 ns, 50ns, and 800 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9 respectively. What is the average access time of the system ignoring the search time within the cache? 4+4

c) 1.ConsiderthefollowingComputer:-

Codetype-	A(1 cycle)	B (2 cycle)	C(3 cycle)
Compiler1	8	7	9
Compiler2	14	3	3

Instruction A requires 2 clock cycles, Instruction B requires 1clock cycle, Instruction C requires 3 clock cycles.
The machine runs at 150 MHz.

(i) Find out MIPS for both the cases and compare them.
(ii) Compare CPU time for both the cases.

2.Define reservation table in pipeline system. 6+2

d) 1.Consider a pipeline with stages S1,S2 and S3 and the following reservation table for a function 'F'. An 'X' indicates that a stage is used at that clock cycle.

Stage	Cycle1	Cycle2	Cycle3	Cycle4
S1	X			X
S2		X	X	
S3			X	

Find out the MAL.

2. Write the difference between loosely coupled and tightly coupled multi process or system. 4+4

Note: Long Questions may be split into Smaller questions according to individual departments or Units but the marks distribution remains the same